REMARKS

Reconsideration and allowance of this application, as amended, is respectfully requested.

This Amendment is in response to the Office Action dated July 9, 2004. By the present Amendment, minor informalities noted in the Abstract have been corrected. Also, the original claims 1-14 have been cancelled, without prejudice, and replaced by new claims 15-28.

With regard to the objection concerning page 1, line 12 of the Specification, Applicants are enclosing herewith in the Appendix a copy of a website for VSI Alliance (VSIA), more specifically, www.vsi.org. As can be seen on the second page of the printout, the statement is made:

> "The pre-designed blocks are a form of Intellectual Property (IP), which is variously referred to as IP, IP blocks, cores, system-level blocks (SLB), ..."

As such, it is respectfully submitted that the use of the term "IP" in referring to Intellectual Property is well known terminology in the art. As such, removal of the objection set forth in paragraph 1 on page 2 of the Office Action is respectfully requested.

With regard to the objection set forth in paragraph 2 in the Office Action, the term CPU has been replaced by "Central Processing Unit" throughout the claims.

Reconsideration and removal of the 35 U.S.C. § 112, second paragraph, rejection set forth in the Office Action is respectfully requested. By the present Amendment, the newly submitted claims 15-28 address each of the issues set forth

in paragraph 7-11 of the Office Action. For example, the "number of clocks" has been revised in the new claims to refer to "clock pulses." The "plurality of functional circuit blocks" has been replaced by "a functional circuit block," with appropriate references throughout the claims. Concerning the original claim 4 (new claim 18), the language has been revised, noting that claim 18 is supported by Fig. 2 (with reference to Fig. 2 being made solely for purposes of example). In particular, claim 18 defines the prediction circuit including a counter (such as CT of Fig. 2), a control circuit (e.g., PD of Fig. 2) and an input detection circuit (e.g., DT of Fig. 2).

With regard to claim 6, new claim 20 replaces claim 6. This claim is supported, for example, by Fig. 3, and defines the elements shown therein.

With regard to claim 8, the term "it" has been deleted in the new corresponding claim 22. It is noted that claim 22 is supported, for example, by the structure shown in Fig. 4.

By virtue of the amendments to these and other claims, it is respectfully submitted that all of the claims 15-28 clearly meet the requirements of 35 U.S.C. § 112, second paragraph. Accordingly, reconsideration and removal of the 5 U.S.C. § 112, second paragraph, rejection is respectfully requested, together with a complete examination on the merits of these claims.

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of either by telephone discussion or by personal interview, the Examiner is invited to contact Applicants' undersigned attorney at the number indicated below.

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Antonelli, Terry, Stout & Kraus, LLP Deposit Account No. 01-2135 (Docket No. 500.40524X00), and please credit any excess fees to such Deposit Account.

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

By _____
Gregory E. Montone
Reg. No. 28,141

GEM/dlt

1300 North Seventeenth Street, Suite 1800
Arlington, Virginia 22209
Telephone: (703) 312-6600
Facsimile: (703) 312-6666

AMENDMENTS TO THE ABSTRACT

Please amend the Abstract as indicated below. A clean version of the Abstract is attached hereto as Appendix A.

ABSTRACT OF THE DISCLOSURE

A semiconductor device having a functional circuit block with predictive power controller is provided so as to construct a system LSI manufactured in ~~the~~a practicable number of design steps, which is extensible and in which power is reduced. The functional circuit block includes a prediction circuit and a predictive power shutdown circuit having a power status control circuit. The prediction circuit controls a power status of the functional circuit block by using the power status control circuit, based on input information thereto. When no information is inputted for a predetermined a period of time, the power status control circuit shifts ~~to~~from a power status of the functional circuit block to a low-power status.

One solution for this dilemma is to design with pre-designed blocks, much as is now done using off-the-shelf ICs on printed circuit boards. The pre-designed blocks are a form of Intellectual Property (IP), which is variously referred to as IP, IP blocks, cores, system-level blocks (SLB), macros, system level macros (SLMs), or Virtual Components (VCs – the VSIA term for these elements).

System Chips

"System Chip" refers to highly integrated devices, which can also be called systems on silicon, systems-on-a-chip, system-on-chip (SoC), system-LSI, system-ASIC, platform ASIC or other similar terms. The definition of what should be included in an SoC varies from analyst to analyst and company to company. But regardless of the nomenclature used or the specific contents, there's no disputing that the trend is rapidly moving toward multi-million-gate devices with more than 80 percent of content determined by pre-designed hardware and software blocks, also called IP cores.

Roadblocks to efficient and economical use of IPs remain. The chief roadblock is the lack of open IP-to-IP interface standards upon which to base IP development and use. Much of the advantage of IP cores is lost if companies must drain resources attempting to recreate data or converting IP formats or interfaces to make them compatible with internal design elements.

With PC boards, there is an infrastructure of standards interfaces, board integration, test, selection and verification of components, etc. This infrastructure allows the mix and match of ICs from different vendors and their rapid integration onto the board.

With system chips, however, there is little infrastructure to support the development and verification of VCs, or the mix and match from multiple sources, or the rapid integration of VCs into a system chip.

System-on-Chip Industry

The system-chip industry includes those who develop the infrastructure for system-chip designs (tools, services, and fabrication) and those who design the system-chip devices themselves, including system and fabless design companies, semiconductor vendors, IP suppliers, and Electronic Design Automation (EDA) vendors, as well as others.

- **Offices and Staff**
- **Standards Philosophy**
- **VSIA Structure**

*The Term IP core is synonymous with Virtual Component (VC), which is also used in VSIA documents.